National Semiconductor

December 1980

DT1050 DIGITALKER™ Standard Vocabulary Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1050 is a standard DIGITALKER kit encoded with 137 separate and useful words, 2 tones, and 5 different silence durations. (See the Master Word List Table I). The words and tones have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences.

The "voice" output of the DT1050 is a highly intelligible male voice. The vocabulary is chosen so that it is applicable to many products and markets.

Features

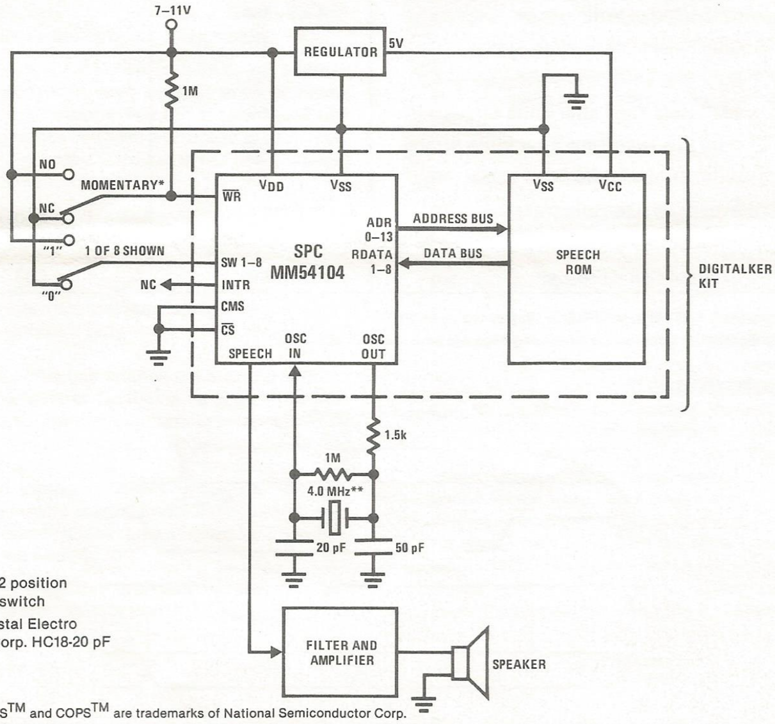
- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- 144 addressable expressions, including numbers
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



* Single pole 2 position momentary switch

** 4.0 MHz crystal Electro Dynamics Corp. HC18-20 pF

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IM-FL30M120/Printed in U.S.A.

Absolute Maximum Ratings*

Storage Temperature Range	−65°C to +150°C	Voltage at Any Pin	12V
Operating Temperature Range	0°C to 70°C	Operating Voltage Range, V_{DD}-V_{SS}	7V to 11V
V_{DD}-V_{SS}	12V	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics* $T_A = 0°C$ to 70°C, $V_{DD} = 7V–11V$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -100\ \mu A$	2.4		5.0	V
V_{ILX}	Clock Input Low Voltage		−0.3		1.2	V
V_{IHX}	Clock Input High Voltage		5.5		V_{DD}	V
I_{DD}	Power Supply Current				45	mA
I_{IL}	Input Leakage				±10	μA
I_{ILX}	Clock Input Leakage				±10	μA
V_S	Silence Voltage			0.45 V_{DD}		V
V_{OUT}	Peak to Peak Speech Output	$V_{DD} = 11V$		2.0		V
R_{EXT}	External Load on Speech Output	R_{EXT} Connected Between Speech Output and V_{SS}	50			kΩ

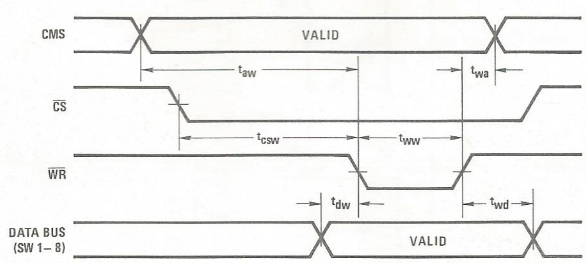
AC Electrical Characteristics* $T_A = 0°C$ to 70°C, $V_{DD} = 7V–11V$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
t_{aw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{wa}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{red}	$\overline{ROMEN}$ ON to Valid ROM Data		2	μs
t_{wss}	Write Strobe to Speech Output Delay		410	μs
f_t	External Clock Frequency	3.92	4.08	MHz

Note: Rise and fall times (10% to 90%) of MICROBUS signals should be 50 ns maximum.
*SPC characteristics only. ROM characteristics covered by separate data sheet for MM52164.

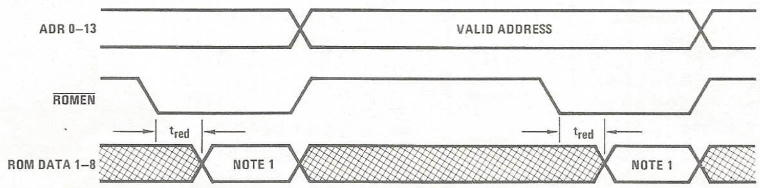
Timing Waveforms

Command Sequence



Timing Waveforms (Continued)

ROM Data Timing



Note 1: ROM Data 1–8 can go valid any time after ADR 0–13 changes, however it must be valid within the t_{red} spec and remain valid until $\overline{ROMEN}$ goes high.

Functional Description

The following describes the function of all SPC input and output pins.

Note: In the following descriptions, a low represents a logic 0 (0.4V nominal), and a high represents a logic 1 (2.4V nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.

Data Bus (SW 1-8): This is an 8-bit parallel data bus which contains the starting address of the speech data.

Data bus inputs SW 1–SW 8 accept an 8-bit binary address which is the address of the word which is to be "spoken" from the DIGITALKER output. See the Master Word List (Table I) for the complete listing of words and their respective addresses. If the entire word list is not used, unused inputs must be connected to V_{SS}.

Command Select (CMS): This line specifies the two commands to the SPC.

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only

Write Strobe ($\overline{WR}$): This line latches the starting address (SW 1–SW 8) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech sequence is issued during a speech sequence, the new speech sequence will be started immediately. When connecting $\overline{WR}$ to a switch, it must be a single pole 2 position switch as shown on page 1.

ROM Data (RDATA 1-8): This is an 8-bit parallel data bus which contains the speech data from the speech ROM.

OUTPUT SIGNALS

Interrupt (INTR): This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.

ROM Address (ADR 0–ADR 13): This is a 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

ROM Enable ($\overline{ROMEN}$): For low power applications, this line can be used to drive a transistor that switches the supply for static speech ROMs. See ROM data timing.

Speech Output (Speech Out): This is the analog output that represents the speech data. See frequency response section.

INPUT/OUTPUT SIGNALS

Clock Input/Output (OSC IN, OSC OUT): These two pins connect the main timing reference (crystal) to the SPC.

PHRASE QUALITY

In normal human speech, the brain puts durations of silence between the words to make the sentence flow smoothly. Since several durations of silence are provided in the Master Word List, the actual quality of any phrase can be significantly improved by adding durations of silence (also assigned addresses) between the words. As one thinks about how the phrase is actually spoken, one might assume the approximate duration of silence between each word, and insert the closest duration of silence from the word list. A hint in this area would be that for words beginning with the letters, K, T, P, B, D, and G insert 80 milliseconds silence prior to the words, and for words ending in the same letters as above, 40 milliseconds silence following the word is recommended.

Functional Description (Continued)

TABLE I. DT1050 MASTER WORD LIST

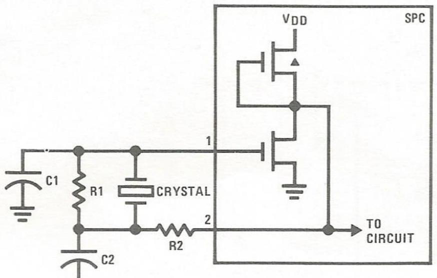
Word	8-Bit Binary Address SW8 … SW1		8-Bit Binary Address SW8 … SW1		8-Bit Binary Address SW8 … SW1
THIS IS DIGITALKER	00000000	Q	00110000	IS	01100000
ONE	00000001	R	00110001	IT	01100001
TWO	00000010	S	00110010	KILO	01100010
THREE	00000011	T	00110011	LEFT	01100011
FOUR	00000100	U	W0110100	LESS	01100100
FIVE	00000101	V	00110101	LESSER	01100101
SIX	00000110	W	00110110	LIMIT	01100110
SEVEN	00000111	X	00110111	LOW	01100111
EIGHT	00001000	Y	00111000	LOWER	01101000
NINE	00001001	Z	00111001	MARK	01101001
TEN	00001010	AGAIN	00111010	METER	01101010
ELEVEN	00001011	AMPERE	00111011	MILE	01101011
TWELVE	00001100	AND	00111100	MILLI	01101100
THIRTEEN	00001101	AT	00111101	MINUS	01101101
FOURTEEN	00001110	CANCEL	00111110	MINUTE	01101110
FIFTEEN	00001111	CASE	00111111	NEAR	01101111
SIXTEEN	00010000	CENT	01000000	NUMBER	01110000
SEVENTEEN	00010001	400HERTZ TONE	01000001	OF	01110001
EIGHTEEN	00010010	80HERTZ TONE	01000010	OFF	01110010
NINETEEN	00010011	20MS SILENCE	01000011	ON	01110011
TWENTY	00010100	40MS SILENCE	01000100	OUT	01110100
THIRTY	00010101	80MS SILENCE	01000101	OVER	01110101
FORTY	00010110	160MS SILENCE	01000110	PARENTHESIS	01110110
FIFTY	00010111	320MS SILENCE	01000111	PERCENT	01110111
SIXTY	00011000	CENTI	01001000	PLEASE	01111000
SEVENTY	00011001	CHECK	01001001	PLUS	01111001
EIGHTY	00011010	COMMA	01001010	POINT	01111010
NINETY	00011011	CONTROL	01001011	POUND	01111011
HUNDRED	00011100	DANGER	01001100	PULSES	01111100
THOUSAND	00011101	DEGREE	01001101	RATE	01111101
MILLION	00011110	DOLLAR	01001110	RE	01111110
ZERO	00011111	DOWN	01001111	READY	01111111
A	00100000	EQUAL	01010000	RIGHT	10000000
B	00100001	ERROR	01010001	SS (Note 1)	10000001
C	00100010	FEET	01010010	SECOND	10000010
D	00100011	FLOW	01010011	SET	10000011
E	00100100	FUEL	01010100	SPACE	10000100
F	00100101	GALLON	01010101	SPEED	10000101
G	00100110	GO	01010110	STAR	10000110
H	00100111	GRAM	01010111	START	10000111
I	00101000	GREAT	01011000	STOP	10001000
J	00101001	GREATER	01011001	THAN	10001001
K	00101010	HAVE	01011010	THE	10001010
L	00101011	HIGH	01011011	TIME	10001011
M	00101100	HIGHER	01011100	TRY	10001100
N	00101101	HOUR	01011101	UP	10001101
O	00101110	IN	01011110	VOLT	10001110
P	00101111	INCHES	01011111	WEIGHT (Note 2)	10001111

Note 1: "SS" makes any singular word plural

Note 2: Address 143 is the last legal address in this particular word list. Exceeding address 143 will produce pieces of unintelligible invalid speech data.

Crystal Circuit Information

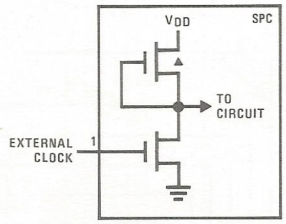
Typical Crystal Oscillator Network

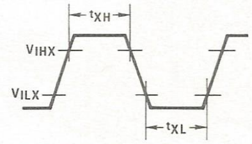


Crystal	R1	R2	C1	C2
4.0 MHz	1M	1.5k	10–30 pF	40–60 pF

(4.0 MHz crystal manufactured by Electro Dynamics Corp. P/N HC18-20 pF)

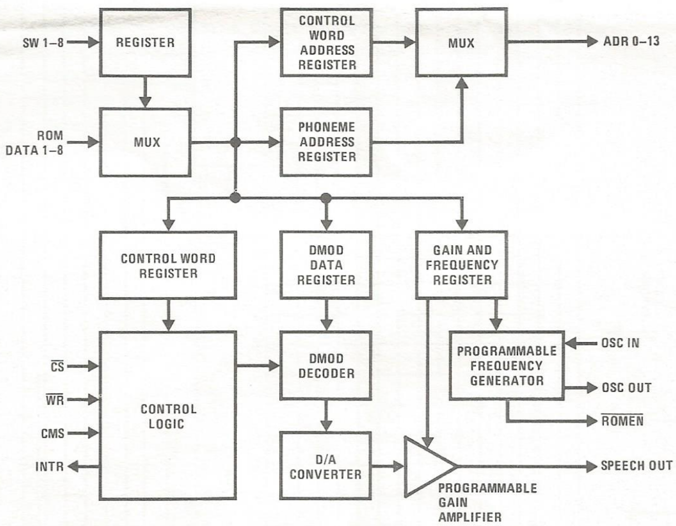
External Clock Input (4.0 MHz)



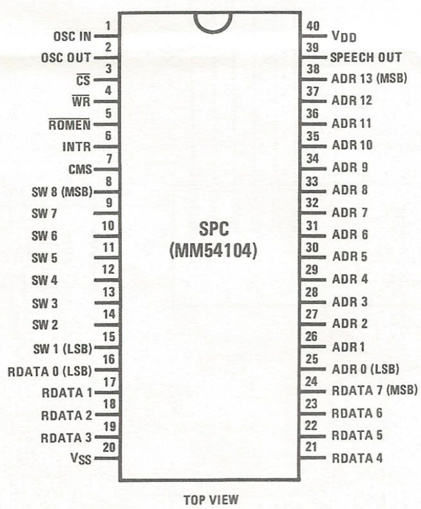


Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

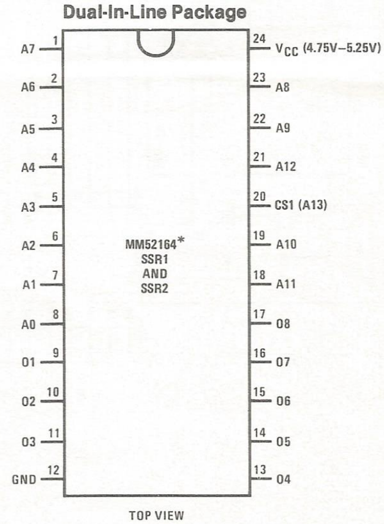
SPC Block and Connection Diagrams



Dual-In-Line Package

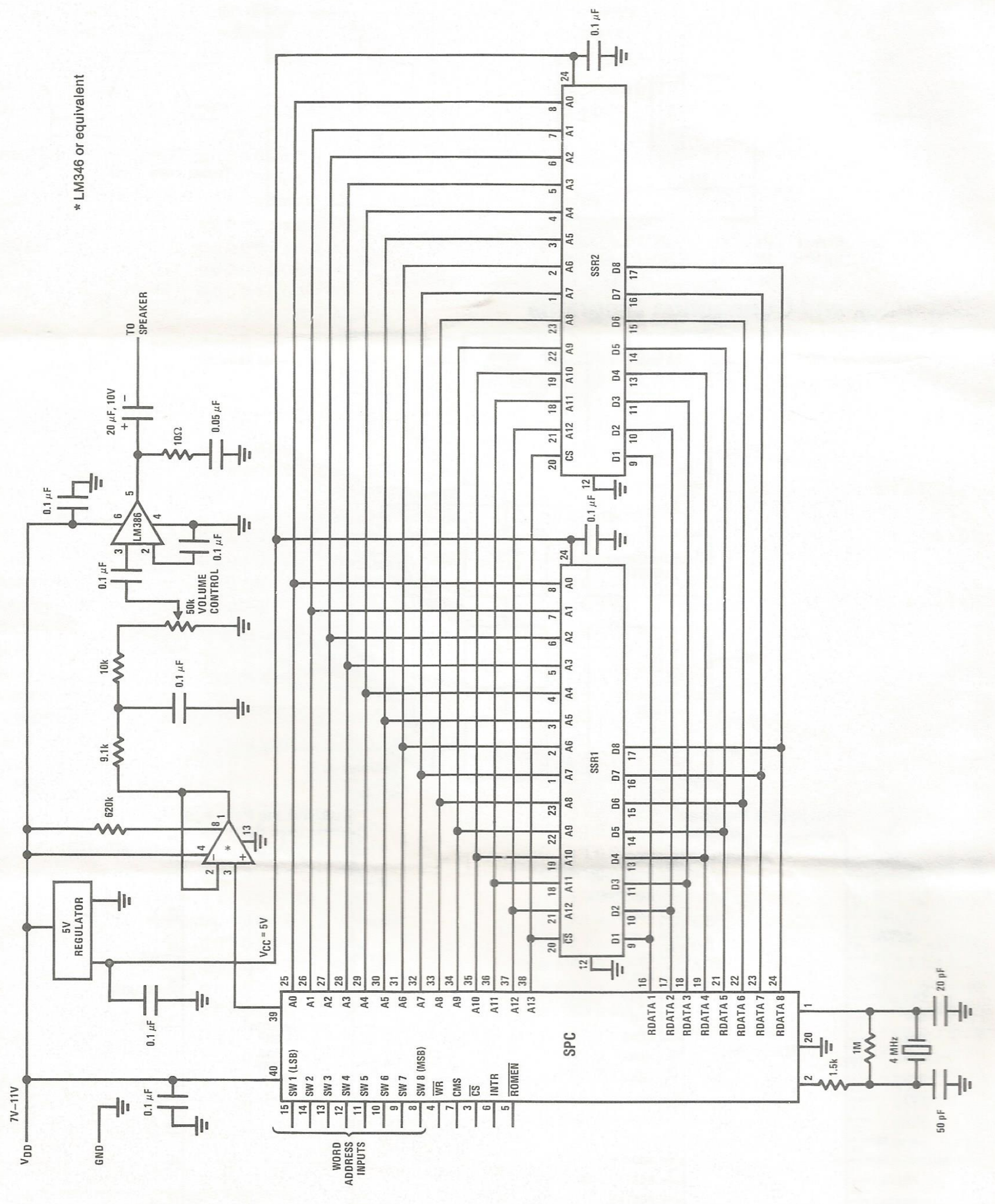


Dual-In-Line Package



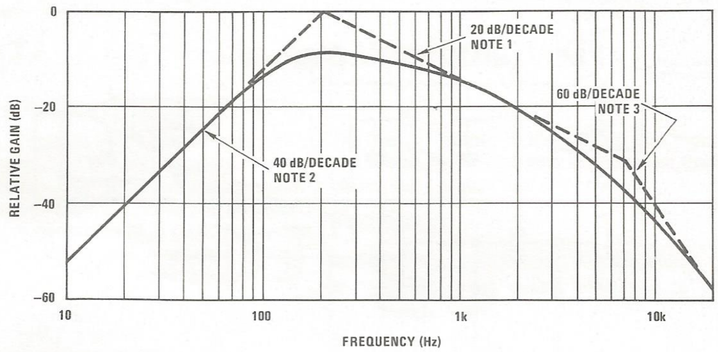
* For specific ROM device information, see MM52164 data sheet.

Recommended Schematic Diagram



Applications Information

Frequency Response of Combined Amplifier and Speaker



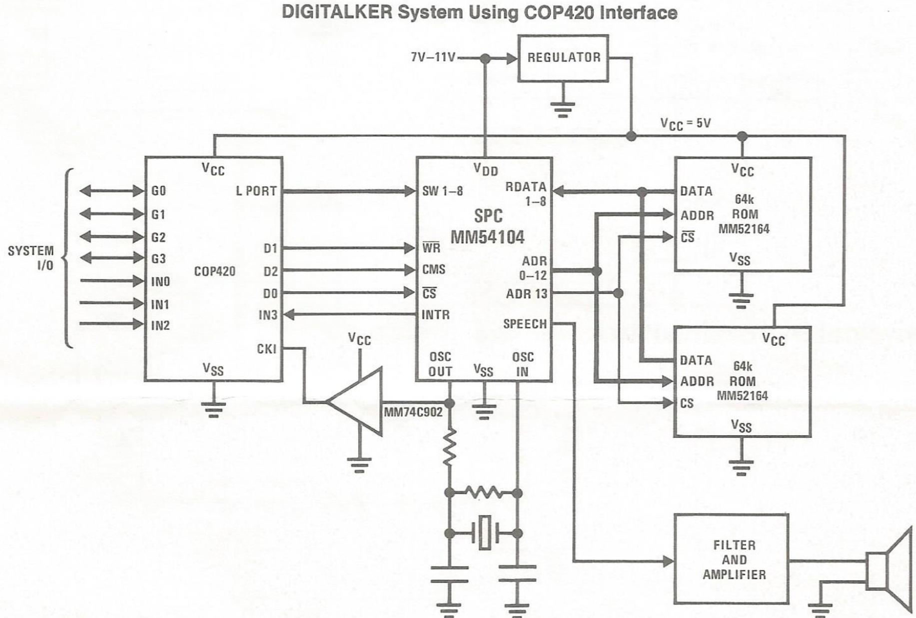
Note 1: This curve is the desired response of the entire audio system including speaker. Minimum response is a low pass filter with a cutoff frequency of 200 Hz. For an audio system with a natural cutoff frequency around 200 Hz, this filter can be eliminated. This cutoff frequency may be tuned for the particular voice being synthesized. For a low pitched male voice it may be 100 Hz, while for a high pitched female or child's voice it might be 300 Hz.

Note 2: This is optional filtering that can be eliminated by proper selection of the speaker. If this 2 pole response is electronically produced, it should be adjusted as described in Note 1.

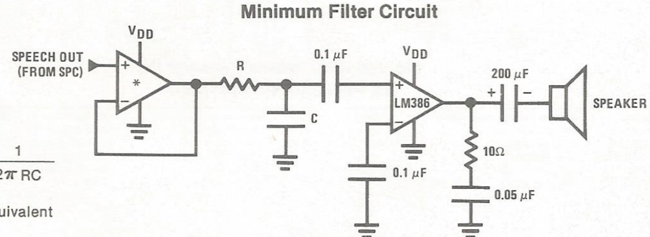
Note 3: This is optional filtering that can be eliminated for simpler systems. The acceptable range for this cutoff frequency is 6000 Hz–8000 Hz.

Typical Applications (Continued)

DIGITALKER System Using COP420 Interface



Minimum Filter Circuit

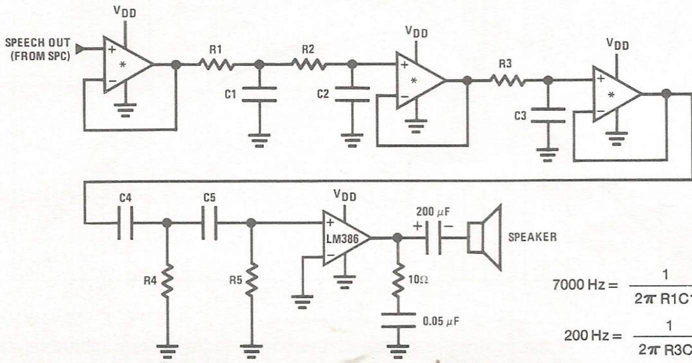


$$200\text{ Hz} = \frac{1}{2\pi RC}$$

* LM346 or equivalent

Typical Applications (Continued)

Filter Circuit to Produce Maximum Frequency Response

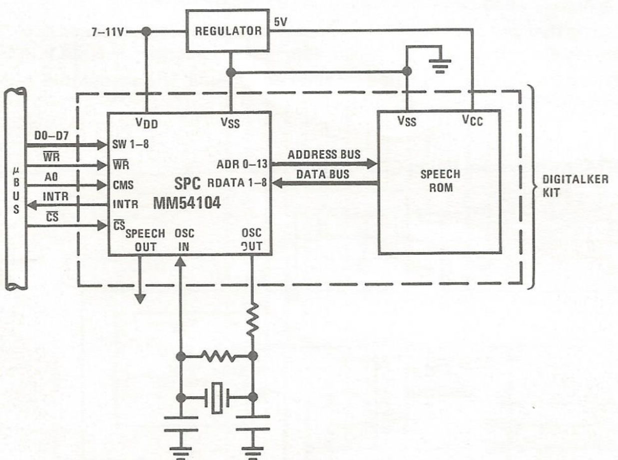


$$7000\text{ Hz} = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

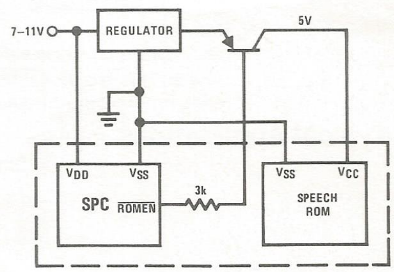
$$200\text{ Hz} = \frac{1}{2\pi R3C3} = \frac{1}{2\pi R4C4} = \frac{1}{2\pi R5C5}$$

* LM346 or equivalent

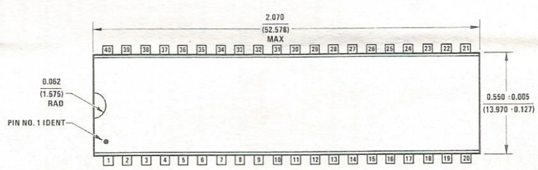
DIGITALKER System Utilizing MICROBUS™ Interface

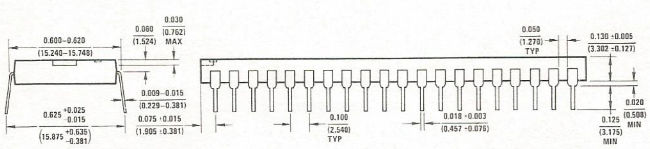


Low Power Configuration Using Static ROM



Physical Dimensions inches (millimeters)





Molded Dual-In-Line Package (N)
NS Package Number N40A

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